1. A data transmission circuit, comprising:

a first bus segment of a data bus;

a second bus segment of said data bus; and

a first switching circuit connected between said first and second segments of said data bus, wherein said first switching circuit is configured to selectively connect said first and second segments of said data bus such that when said first switching circuit is in a first state, said first switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said first switching circuit is in a second state, said second bus segment is disconnected from said first bus segment and data is passed through from said first bus segment to at least one I/O circuit and from said at least one I/O circuit to said first bus segment.

2. A data transmission circuit as in claim 1, further comprising a second switching circuit connected between said second segment of said data bus and a third segment of said data bus, wherein said second switching circuit is configured to selectively connect said second and third segments of said data bus such that when said second switching circuit is in a first state, said second switching circuit passes data through from said second bus segment to said third bus segment and from said third bus segment to said second bus segment, and when said second switching circuit is in a second state, said third bus segment is disconnected from said second bus segment and data is passed through from said second bus segment

to at least one I/O circuit and from said at least one I/O circuit to said second bus segment.

3. A data transmission circuit as in claim 2, further comprising a plurality of switching circuits each configured to selectively pass data between segments of said data bus when in said first state, and between a segment of said data bus and at least one I/O circuit when in said second state.

4. A data transmission circuit as in claim 1, wherein said first switching circuit includes a two-way switch that couples said first and second bus segments when said switching circuit is in said first state, and couples said first bus segment to said at least one I/O circuit when said switching circuit is in said second state.

5. A data transmission circuit as in claim 1, wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on a command and address bus.

6. A data transmission circuit as in claim 1, wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on said data bus.

7. A data transmission circuit as in claim 1, wherein said first switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on at least one dedicated selection data path.

8. A data transmission circuit as in claim 1, wherein said data bus is a multidrop bus.

9. A data transmission circuit as in claim 1, wherein said data bus is a substantially stubless data bus.

10. A data transmission circuit as in claim 1, wherein said first switching circuit includes a p-channel field-effect transistor (FET) switch.

11. A data transmission circuit as in claim 1, wherein said first switching circuit includes a p-channel field-effect transistor (FET) switch and an n-channel FET switch.

12. A data transmission circuit as in claim 1, wherein said first switching circuit is formed using Gallium Arsenide (GaAs) semiconductor technology.

13. A data transmission circuit as in claim 1, wherein said first switching circuit has a programmable drive strength.

14. A data transmission circuit as in claim 1, wherein said first switching circuit is located on a motherboard.

15. A data transmission circuit as in claim 1, wherein said first switching circuit is located on a memory module.

16. A data transmission circuit as in claim 1, wherein said first switching circuit is located on a same integrated circuit chip as a memory device.

17. A data transmission circuit as in claim 1, wherein said first switching circuit receives a command selecting at least one attached I/O circuit for point-to-point communications, selects said second state of said first switching circuit to disconnect said first bus segment from said second bus segment, and passes data between said first bus segment and said at least one attached selected I/O circuit.

18. A data transmission circuit as in claim 1, wherein said data bus is a first data bus having a first number of data paths, and said first switching circuit is further configured to connect to a second data bus having a second number of data paths, wherein said first switching circuit is connected between said first and second data buses for selectively receiving data on said first data bus and placing said data on said second data bus and selectively receiving data on said second data bus and placing said data on said first data bus.

19. A data transmission circuit as in claim 18, wherein said first switching circuit performs a data rate conversion between said first and second data buses.

20. A data transmission circuit as in claim 19, wherein said first switching further comprises at least one of a multiplexer and demultiplexer for performing said data rate conversion.

21. A data transmission circuit as in claim 18, wherein said first switching circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

22. A data transmission circuit as in claim 18, wherein said first switching circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

23. A data transmission circuit as in claim 18, wherein said first number of data paths is less than said second number of data paths.

24. A data transmission circuit as in claim 18, wherein said second data bus is connected to said at least one I/O circuit.

25. A data transmission circuit as in claim 24, wherein said at least one I/O circuit includes a programmable bus terminator.

26. A data transmission circuit as in claim 18, wherein said first data bus is connected to a memory controller.

27. A data transmission circuit as in claim 26, wherein said memory controller includes a programmable bus terminator.

28. A data transmission circuit as in claim 18, wherein said first data bus is connected to a processor.

29. A data transmission circuit as in claim 18, wherein said first switching circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins.

30. A data transmission circuit as in claim 29, wherein said data transmission circuit comprises a plurality of said switching circuits connected between said first and second segments of said first data bus via said first and second sets of I/O pins.

31. A data transmission circuit as in claim 18, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

32. A data transmission circuit as in claim 18, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

33. A data transmission circuit as in claim 18, wherein said first data bus transmits analog signals.

34. A data transmission circuit as in claim 18, wherein said first data bus transmits digital signals.

35. A data transmission circuit as in claim 18, wherein said first data bus transmits radio-frequency (RF) signals.

36. A data transfer interface, comprising:

a first bus segment of a data bus;

a second bus segment of said data bus; and

an interface circuit connected between said first and second segments of said data bus, wherein said interface circuit includes a switching circuit configured to selectively connect said first and second segments of said data bus such that when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said data bus and said second bus segment is disconnected from said first bus segment.

37. An interface as in claim 36, wherein when said switching circuit is in said first state, said interface circuit does not receive or transmit data on said data bus.

38. An interface as in claim 36, wherein when said switching circuit is in said second state, said interface circuit receives and transmits data using said first segment of said data bus in a point-to-point data communications configuration.

39. An interface as in claim 36, wherein said switching circuit includes a field effect transistor (FET) switch.

40. An interface as in claim 39, wherein said FET switch includes a p-channel transistor.

41. An interface as in claim 36, wherein said switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on a command and address bus.

42. An interface as in claim 36, wherein said switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on said data bus.

43. An interface as in claim 36, wherein said switching circuit selectively connects said first and second segments of said data bus according to a selection signal received on at least one dedicated selection data path.

44. An interface as in claim 36, wherein said data bus is a multidrop bus.

45. An interface as in claim 36, wherein said data bus is a substantially stubless data bus.

46. An interface as in claim 36, wherein said interface circuit receives a command selecting the interface circuit for point-to-point communications, selects

said second state of said switching circuit to disconnect said first bus segment from said second bus segment, and performs at least one of receiving and transmitting data on said data bus using said first bus segment.

47. An interface as in claim 36, wherein said data bus is a first data bus having a first number of data paths, and further comprising a second data bus having a second number of data paths, wherein said interface circuit is connected between said first and second data buses for selectively receiving data on said first data bus and placing said data on said second data bus and selectively receiving data on said second data bus and placing said data on said first data bus.

48. An interface as in claim 47, wherein said interface circuit performs a data rate conversion between said first and second data buses.

49. An interface as in claim 48, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer for performing said data rate conversion.

50. An interface as in claim 47, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

51. An interface as in claim 47, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

52. An interface as in claim 47, wherein said first number of data paths is less than said second number of data paths.

53. An interface as in claim 47, wherein said second data bus is connected to at least one memory device.

54. An interface as in claim 47, wherein said first data bus is connected to a memory controller.

55. An interface as in claim 47, wherein said first data bus is connected to a processor.

56. An interface as in claim 47, wherein said interface circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins, and I/O pins of said first set are connected to respective I/O pins of said second set through said switching circuit.

57. An interface as in claim 47, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

58. An interface as in claim 47, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

59. An interface as in claim 47, wherein said first data bus transmits analog signals.

60. An interface as in claim 47, wherein said first data bus transmits digital signals.

61. An interface as in claim 47, wherein said first data bus transmits radio-frequency (RF) signals.

62. An interface as in claim 47, wherein said interface circuit selects data for receipt and transmission on said first data bus according to a selection signal received on a command and address bus.

63. An interface as in claim 62, wherein said selection signal controls said switching circuit, whereby said first segment is disconnected from said second segment while data is being received and transmitted on said first data bus.

64. A memory module, comprising:

at least one memory device; and

a data transfer interface for connection to a segmented data bus, said data transfer interface being coupled to said at least one memory device and comprising:

a first segment of said data bus;

a second segment of said data bus; and

an interface circuit configured for connection between said first and second segments of said data bus, wherein said interface circuit includes a switching circuit configured to selectively connect said first and second segments of said data bus such that when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said data bus and said second bus segment is disconnected from said first bus segment.

65. A memory system, comprising:

at least one memory device; and

a data transfer interface connected to a first segmented data bus and to said at least one memory device by a second data bus, said data transfer interface comprising:

a first segment of said first data bus;

a second segment of said first data bus; and

an interface circuit connected between said first and second segments of said first data bus, wherein said interface circuit includes a switching circuit configured to selectively connect said first and second segments of said first data bus such that

when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said first data bus and said second bus segment is disconnected from said first bus segment.

66. A memory system as in claim 65, wherein said at least one memory device is included in a memory module.

67. A memory system as in claim 65, wherein said switching circuit includes a field effect transistor (FET) switch.

68. A memory system as in claim 67, wherein said FET switch includes a p-channel transistor.

69. A memory system as in claim 65, wherein said interface circuit further comprises at least one conversion circuit which performs a data rate conversion between said first and second data buses.

70. A memory system as in claim 69, wherein said at least one conversion circuit comprises at least one of a multiplexer and demultiplexer.

71. A memory system as in claim 65, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

72. A memory system as in claim 65, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

73. A memory system as in claim 65, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

74. A memory system as in claim 65, wherein said first number of data paths is less than said second number of data paths.

75. A memory system as in claim 65, wherein said first data bus is connected to a memory controller.

76. A memory system as in claim 65, wherein said first data bus is connected to a processor.

77. A memory system as in claim 65, wherein said interface circuit is connected to said first bus segment of said first data bus via a first set of I/O pins and to said second bus segment via a second set of I/O pins, and I/O pins of said first set are connected to respective I/O pins of said second set through said switching circuit.

78. A memory system as in claim 65, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

79. A memory system as in claim 65, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

80. A memory system as in claim 65, wherein said first data bus transmits analog signals.

81. A memory system as in claim 65, wherein said first data bus transmits digital signals.

82. A memory system as in claim 65, wherein said first data bus transmits radio-frequency (RF) signals.

83. A memory system as in claim 65, wherein said interface circuit selects data for receipt from said first data bus according to a selection signal received on a command and address bus.

84. A memory system as in claim 83, wherein said selection signal controls said switching circuit, whereby said first segment is disconnected from said second segment while data is being received from said first data bus.

85. A memory system as in claim 65, wherein said interface circuit is further configured to selectively receive data on said second data bus and place said data on said first data bus.

86. A memory system as in claim 65, wherein said interface circuit selects data for receipt from said second data bus according to a selection signal received on a command and address bus.

87. A memory system as in claim 86, wherein said selection signal controls said switching circuit, whereby said first segment is disconnected from said second segment while data is being placed on said first data bus.

88. A memory system as in claim 65, wherein said first data bus is a multidrop bus.

89. A memory system as in claim 65, wherein said first data bus is a substantially stubless data bus.

90. A data exchange system, comprising:

a data bus having a plurality of bus segments; and

a plurality of system devices each connected to said first data bus, at least one of said system devices including a switching circuit connected between first and second bus segments of said data bus for selectively passing data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and for selectively disconnecting said second bus segment from said first bus segment to permit point-to-point data communications between said at least one system device and another system device using one of said first and second bus segments.

91. A system as in claim 90, wherein said switching circuit includes a field effect transistor (FET) switch.

92. A system as in claim 91, wherein said FET switch includes a p-channel transistor.

93. A system as in claim 90, wherein said plurality of system devices includes a processor.

94. A system as in claim 90, wherein said plurality of system devices includes a memory controller.

95. A system as in claim 90, wherein said plurality of system devices includes a bus terminator.

96. A system as in claim 90, wherein said plurality of system devices includes a memory module.

97. A system as in claim 90, wherein said plurality of system devices includes a memory device.

98. A system as in claim 90, wherein said plurality of system devices includes an interface circuit for communication with other system devices connected to a second data bus.

99. A system as in claim 90, wherein a switchable terminator is included in at least one of said plurality of system devices.

100. A system as in claim 90, wherein a programmable terminator is included in at least one of said plurality of system devices.

101. A processor system comprising;

a processor;

at least one memory subsystem connected to said processor; and

a segmented bus which connects each of a controller and at least one memory subsystem interface circuit of said at least one memory subsystem;

whereby said memory subsystem interface circuit couples at least one memory device to said segmented bus, said memory subsystem interface circuit including a conversion circuit and a switching circuit, said conversion circuit receiving data from said segmented bus, converting it to data which can be processed by said at least one memory device, receiving data from said at least one memory device and converting it to data which can be transmitted over said segmented bus, said switching circuit being connected between first and second bus segments of said segmented bus such that when said switching circuit is in a first state, said switching circuit passes data through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, and when said switching circuit is in a second state, said interface circuit receives and transmits data on said first data bus and said second bus segment is disconnected from said first bus segment.

102. A system as in claim 101, wherein said switching circuit includes a field effect transistor (FET) switch.

103. A system as in claim 102, wherein said FET switch includes a p-channel transistor.

104. A system as in claim 101, wherein said controller resides on a same printed circuit board as said processor.

105. A system as in claim 101, wherein said controller is integrated into said processor.

106. A method of data communication between devices in an electronic circuit, comprising:

connecting at least one switching circuit between segments of a data bus;

selectively passing data on said data bus through from a first bus segment to a second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using said switching circuit, whereby when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments.

107. A method as in claim 106, wherein said selective passing of data includes configuring said at least one switching circuit to pass data during WRITE operations.

108. A method as in claim 106, wherein said selective passing of data includes configuring said at least one switching circuit to pass data between a memory controller and a selected I/O device during READ operations.

109. A method as in claim 106, wherein said selective passing of data includes configuring said at least one switching circuit to pass data between a memory controller and a selected I/O device during WRITE operations.

110. A method of data communication between devices in an electronic circuit, comprising:

connecting a first set of I/O pins of an interface circuit to a first segment of a data bus;

connecting a second set of I/O pins of said interface circuit to a second segment of said data bus;

receiving and transmitting data on at least said first segment of said data bus using at least said first set of I/O pins; and

selectively passing data on said data bus through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using a switching circuit.

111. A method as in claim 110, wherein when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments.

112. A method of data communication between devices in an electronic circuit, comprising:

connecting an interface circuit having first and second sets of I/O pins to respective first and second segments of a first data bus that operates at a first data rate;

connecting said interface circuit to a second data bus that operates at a second data rate;

receiving and transmitting data on said first data bus using said first and second sets of I/O pins;

receiving and transmitting data on said second data bus;

selectively converting data received from one of said first and second data buses for use on the other of said first and second data buses; and

selectively passing data on said first data bus through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment, said selective passing of data being performed using a switching circuit, whereby when said data passing is not selected said switching circuit disconnects said first bus segment from said second bus segment to permit point-to-point data communications using one of said first and second bus segments.

113. A method as in claim 112, wherein said selectively converting data includes using a selection signal to determine whether to convert for use on the other of said first and second data buses.

114. A method as in claim 113, wherein said selective conversion of data is performed when said interface circuit is selected for operation by said selection signal.

115. A method as in claim 113, wherein said selective conversion of data is not performed when said interface circuit is not selected for operation by said selection signal.

116. A method as in claim 112, wherein said first data rate is faster than said second data rate.

117. A method as in claim 112, further comprising converting received data between said first data rate of said first data bus and said second data rate of said second data bus.

118. A method as in claim 112, further comprising converting received data between a first encoding of said first data bus and a second encoding of said second data bus.

119. A method as in claim 112, further comprising converting received data between a first voltage level of said first data bus to a second voltage level of said second data bus.

120. A method as in claim 119, wherein said first voltage level is less than said second voltage level.

121. A method as in claim 112, wherein said first data bus connects to said first and second sets of I/O pins using a first bus width different from a second bus width used to connect said interface circuit to said second data bus.

122. A method as in claim 121, wherein said first bus width is less than said second bus width.

123. A method as in claim 112, wherein devices of a first technology communicate with said interface circuit using said first data bus and devices of a second technology communicate with said interface circuit using said second data bus.

124. A method as in claim 123, wherein said devices of said first technology include at least one processor.

125. A method as in claim 123, wherein said devices of said second technology include at least one memory device.

126. A method as in claim 112, wherein said first data bus is a multi-drop bus.

127. A method as in claim 112, wherein said first data bus is a substantially stubless data bus.